WHAT IS CLAIMED IS:

1. A method of generating the design of an integrated circuit using a description language, comprising the acts of:

editing a first file specific to the design;

defining the location of at least one library file;

generating a script using said first file, said library file, and user input information;

running said script to create a customized description language model; and

synthesizing said design based on said description language model.

2. The method of Claim 1, wherein said description language comprises a hardware description language (HDL).

3. The method of Claim 1, wherein the act of synthesizing comprises running synthesis scripts based on said customized description language model.

4. The method of Claim 1, further comprising the act of generating a second file for use with a simulation, and simulating said design using said second file.

5. The method of Claim 4, further comprising the act of evaluating the acceptability of the design based on said simulation.

6. The method of Claim 5, further comprising the acts of revising the design to produce a revised design, and re-synthesizing said revised design.

7. The method of Claim 1, wherein the act of editing comprises selecting a plurality of input parameters associated with said design, said parameters comprising:

(i) at least one custom instruction;

(ii) a cache configuration; and

(iii) a memory interface configuration.

8. A description language model of an integrated circuit design generated using the method comprising:

editing a first file specific to said integrated circuit design;

defining the location of at least one library file;

generating a script using said first file, said library file, and user input information; and

running said script to create said description language model of said integrated circuit design.

9. The model of Claim 8, wherein the act of editing comprises selecting a plurality of input parameters associated with said design, said parameters comprising:

(i) at least one custom instruction set;

(ii) a cache configuration; and

(iii) a memory interface configuration.

10. The model of Claim 8, wherein said description language comprises VHDL.

11. The model of Claim 9, wherein the act of selecting further comprises selecting each of said plurality of parameters from a plurality of options presented by a menu-driven computer program.

12. An integrated circuit, fabricated using the method comprising:

editing a first file specific to a desired integrated circuit design;

defining the location of at least one library file;

generating a script using said first file, said library file, and user input information;

running said script to create a customized description language model of said integrated circuit design;

generating a netlist which is descriptive of the circuitry of said integrated circuit;

compiling said netlist and said hardware description model to produce a compiled integrated circuit design;

fabricating at least one mask representing said compiled integrated circuit design; and

fabricating said integrated circuit using said at least one mask.

13. The integrated circuit of Claim 12, wherein the act of editing comprises selecting at least one of a plurality of input parameters associated with said design, said at least one parameter being selected from the group comprising:

(i) custom instruction sets;

(ii) cache configurations;

(iii) memory interface configurations; and

(iv) system architecture configurations.

14. The integrated circuit of Claim 12, wherein the act of generating a netlist comprises generating a list of logic devices and their interconnections.

15. The integrated circuit of Claim 12, wherein the act of fabricating said integrated circuit comprises defining physical features on a semi-conductive substrate via a lithographic process.

16. The integrated circuit of Claim 12, further comprising synthesizing said design based on said description language model.

17. The integrated circuit of Claim 13, wherein the act of editing is performed interactively with the user using a display.

18. An apparatus adapted to generate integrated circuit designs, comprising;

a processor capable of running a computer program;

a storage device operatively coupled to said processor, said storage device being capable of storing at least a portion of a computer program;

an input device, operatively coupled to said processor, capable of receiving input from a user and transmitting said input to said processor; and

a computer program resident at least in part on said storage device, said computer program adapted to receive said input from said user and perform the following acts based on said input:

editing a first file specific to said integrated circuit design;

defining the location of at least one library file;

generating a script using said first file, said library file, and user input information; and

running said script to create said description language model of said integrated circuit design.

19. The apparatus of Claim 18, wherein said description language model is a hardware description language (HDL).

20. The apparatus of Claim 18, wherein said computer program is further adapted to perform the acts comprising:

generating a second file based on said description language model for use with a simulation; and

simulating said design using said second file.

21. The apparatus of Claim 20, wherein said computer program is further adapted to perform the act comprising running synthesis scripts based on said description language model in order to synthesize said integrated circuit design.

22. The apparatus of Claim 18, wherein said processor comprises a digital microprocessor, and said storage device comprises magnetic media.

23. A system adapted for interactively generating an integrated circuit design based on inputs received from a user, comprising:

a computer having a processor and an input device; and

a computer program capable of running on said processor, said computer program comprising:

a first algorithm having a plurality of user-selectable files, said user-selectable files comprising;

a first file comprising at least one instruction;

a second file comprising a plurality of cache configurations; and

a third file comprising a plurality of memory interface configurations;

a second algorithm capable of generating a script based on selections made by said user from said first, second, and third files and input to said computer program via said input device; and

a third algorithm capable of running said script to generate a description language model of said integrated circuit design.

24. The system of Claim 23, wherein said program is embodied in object code and stored on a storage device accessible by said processor.

25. The system of Claim 24, wherein said storage device is a rotating media magnetic storage device.

26. The system of Claim 23, said first algorithm further comprising a fourth user-selectable file, said fourth file comprising a plurality of system architectures.

27. The system of Claim 23, further comprising a fourth algorithm capable of simulating said integrated circuit design based on said description language model.

28. A method of generating an integrated circuit design, comprising:

providing a user with a plurality of optional instructions;

selecting at least one of said plurality of optional instructions;

selecting at least one cache configuration;

defining at least one memory interface;

generating a script based on said at least one optional instruction, cache configuration, and memory interface; and

running said script to generate a hardware description language model of said integrated circuit design.

29. The method of Claim 28, further comprising the act of selecting at least one synthesis library.

30. The method of Claim 28, wherein the act of providing further comprises allowing the user to generate a customized optional instruction

31. The method of Claim 28, further comprising:

synthesizing said design using said hardware description language model; and

simulating said design using said hardware description language model.

32. The method of Claim 28, wherein the act of selecting at least one of said optional instructions comprises selecting a mathematical operation to be performed on the data resident in at least one data register.

33. The method of Claim 31, wherein the act of simulating said design comprises generating a makefile.

34. The method of Claim 28, further comprising selecting a process technology as the basis for the design.

35. An integrated circuit, comprising:

a microprocessor core; and

a memory operatively coupled to said microprocessor;

wherein said integrated circuit is designed using the method comprising:

selecting the cache size;

defining the memory interface configuration;

selecting at least one customized instruction;

defining the location of at least one library file;

generating a script based on said cache size, memory interface configuration, at least one customized instruction, and said library file;

running said script to create a customized hardware description language model of the design; and

running a synthesis algorithm to synthesize a file descriptive of said design.

36. The integrated circuit of Claim 35, further comprising a digital signal processor (DSP) core, said DSP core being in data communication with said microprocessor and said memory.

37. The integrated circuit of Claim 35, wherein said cache size is a non-zero number of bytes, and said memory interface configuration defines at least one byte of random access memory space.

38. The integrated circuit of Claim 35, wherein said method further comprises the act of selecting a process technology to be used for the design.

39. The integrated circuit of Claim 38, wherein said process technology is a 0.18 micron process.

40. A system for generating integrated circuit designs, comprising:

a processor;

a storage device in data communication with said processor, said storage device being capable of storing and retrieving a computer program; and

a computer program stored within said storage device and adapted to run on said processor, said computer program comprising;

a user-configurable macro-instruction having at least a first user-selectable element, said first-selectable element being selected from the group comprising;

(i) a plurality of custom instructions;

(ii) a plurality of cache configurations;

(iii) a plurality of memory interface configurations; and

(iv) a plurality of system architecture configurations;

a first algorithm capable of generating a script based on selections made by a user from said at least first user selectable element; and

a second algorithm capable of running said script to generate a description language model of an integrated circuit design.

41. The system of Claim 40, wherein said computer program further comprises a second user-selectable element, said second user-selectable element allowing said user to select one of a plurality of process technology options.

42. The system of Claim 40, wherein said first user-selectable element is selected by the act of reading a pre-configured data file.

43. A data storage device adapted for use with a computer, comprising:

data storage media, said data storage media capable of storing a plurality of data bytes; and

a computer program stored as a plurality of data bytes on said data storage media, said computer program comprising:

a first algorithm having a plurality of user-selectable files, said user-selectable files comprising;

a first file comprising at least one functional instruction; and

a second file comprising a plurality of memory interface configurations;

a second algorithm capable of generating a script based on selections made by said user from said first and second files; and

a third algorithm capable of running said script to generate a description language model of said integrated circuit design.

44. The storage device of Claim 43, wherein said storage media comprises a rotating magnetic disk, and said computer program comprises object code stored on said storage media.

45. The storage device of Claim 43, wherein said first algorithm further comprises:

a third file comprising a plurality of cache configurations;

a fourth file comprising a plurality of system architectures; and

a fifth file comprising a plurality of process technology options.

46. A data storage device, comprising:

a storage media capable of storing a plurality of data files; and

a computer program stored as at least one data file on said data storage media, said computer program comprising:

a user-configurable macro-instruction having at least one user-selectable element, said user-selectable element being selected from the group comprising;

(i) a plurality of instructions;

(ii) a plurality of cache configurations;

(iii) a plurality of memory interface configurations; and

(iv) a plurality of system architecture configurations;

a first algorithm capable of generating a script based on selections made by said user from said user-configurable macro-instruction; and

a second algorithm capable of running said script to generate a description language model of an integrated circuit design.

47. A method of generating the design of an integrated circuit using a hardware description language, comprising the acts of:

selecting a process technology;

editing a first file specific to the design, said act of editing comprising selecting at least one user-configurable parameter selected from the group comprising;

(i) processor instructions;

(ii) cache configuration;

(iii) memory interface configuration; and

(iv) system architecture configuration;

defining the location of at least one library file;

generating a script using said first file and said library;

running said script to create a customized hardware description language model of the design; and

running a synthesis algorithm to synthesize a file descriptive of said design.

48. A system for generating integrated circuit designs, comprising:

means for processing digital data;

means for data storage in data communication with said processor means, said means for data storage being capable of storing and retrieving a computer program; and

a computer program stored within said means for data storage and adapted to run on said processor means, said computer program comprising;

means for selecting a process technology;

a user-configurable macro-instruction having at least one user-selectable element, said user-selectable element being selected from the group comprising;

(i) a plurality of instructions;

(ii) a plurality of cache configurations;

(iii) a plurality of memory interface configurations; and

(iv) a plurality of system architecture configurations;

means for generating a script based on said user selectable element and said process technology; and

means for running said script to generate a description language model of an integrated circuit design.

49. A sub-micron feature integrated circuit, comprising:

a microprocessor core having a program bus and data bus;

at least one cache memory; and

a random access memory (RAM) operatively coupled to said microprocessor;

wherein said integrated circuit is synthesized using the following steps performed interactively during the design process:

selecting the size of said cache;

defining the configuration of the interface with said RAM;

selecting at least one customized instruction performed by said microprocessor core;

defining the location of at least one library file;

generating a script based on said size of said cache, said RAM interface configuration, said at least one customized instruction, and said at least one library file;

running said script to create a customized hardware description language model of the design; and

running a synthesis algorithm to synthesize a file descriptive of said design;

wherein said microprocessor core, said program and data busses, said RAM, and said cache are all physically located on the same die.

50. A sub-micron feature integrated circuit, comprising:

a microprocessor core having a program bus and data bus; and

a random access memory (RAM) operatively coupled to said microprocessor;

wherein said integrated circuit is synthesized using the following steps performed interactively during the design process:

defining the configuration of the interface with said RAM;

selecting at least one customized instruction performed by said microprocessor core;

defining the location of at least one library file;

generating a script based on said size of said cache, said RAM interface configuration, said at least one customized instruction, and said at least one library file;

running said script to create a customized hardware description language model of the design; and

running a synthesis algorithm to synthesize a file descriptive of said design;

wherein said microprocessor core, said program and data busses, said RAM, and said cache memory are all physically located on the same die.

51. An integrated circuit, fabricated using the method comprising:

editing a first file specific to a desired integrated circuit design;

defining the location of at least one library file;

generating a script using said first file, said library file, and user input information;

running said script to create a customized description language model of said integrated circuit design;

generating a netlist which is descriptive of the circuitry of said integrated circuit;

compiling said netlist and said hardware description model to produce a compiled integrated circuit design;

compiling at least one configuration file, and

fabricating said integrated circuit using said configuration file;

wherein the act of fabricating further comprises programming a field programmable gate array (FPGA) using said configuration file.

52. A method of generating a design language representation of an integrated circuit, comprising the acts of:

obtaining user input information;

identifying at least one library file;

generating a script using at least said library file and user input information; and

running said script to create a customized description language model.

53. A description language model of an integrated circuit design generated using the method comprising:

obtaining user input information;

identifying at least one library file;

generating a script using said said library file and user input information; and

running said script to create said description language model of said integrated circuit design.

54. An integrated circuit, comprising:

a processor core; and

a memory operatively coupled to said microprocessor;

wherein said integrated circuit is designed using the method comprising:

selecting the cache size;

determining the memory interface configuration;

selecting at least one customized instruction;

identifying at least one library;

generating a script based at least on said cache size, memory interface configuration, at least one customized instruction, and said library; and

running said script to create a customized hardware description language model of the design.

55. A system for generating integrated circuit designs, comprising:

a processor;

a storage device in data communication with said processor, said storage device being capable of storing and retrieving a computer program; and

a computer program stored within said storage device and adapted to run on said processor, said computer program comprising;

a user-configurable macro-instruction having at least a first user-selectable element, said first-selectable element being selected from the group consisting of;

(i) a plurality of custom instructions;

(ii) a plurality of cache configurations;

(iii) a plurality of memory interface configurations; and

(iv) a plurality of system architecture configurations;

a first algorithm capable of generating a script based on selections made by a user from said at least first user selectable element; and

a second algorithm capable of running said script to generate a description language model of an integrated circuit design.

56. A data storage device, comprising:

storage media capable of storing a plurality of data files; and

a computer program stored on said data storage media, said computer program comprising:

a user-configurable macro-instruction having at least one user-selectable element, said user-selectable element being selected from the group consisting of;

(i) a plurality of instructions;

(ii) a plurality of cache configurations;

(iii) a plurality of memory interface configurations; and

(iv) a plurality of system architecture configurations;

a first algorithm capable of generating a script based on selections made by said user from said user-configurable macro-instruction; and

a second algorithm capable of running said script to generate a description language model of an integrated circuit design.

57. A method of generating the design of an integrated circuit using a hardware description language, comprising the acts of:

selecting a process technology;

editing first data specific to the design, said act of editing comprising selecting at least one user-configurable parameter selected from the group consisting of;

(i) processor instructions;

(ii) cache configuration;

(iii) memory interface configuration; and

(iv) system architecture configuration;

identifying at least one library;

generating a script using said first data and said library; and

running said script to create a customized hardware description language model of the design.

58. A sub-micron feature integrated circuit, comprising:

a microprocessor core having a program bus and data bus;

at least one cache memory; and

a random access memory (RAM) operatively coupled to said microprocessor;

wherein said integrated circuit is created using the following steps performed interactively during the design process:

selecting the size of said cache;

defining the configuration of the interface with said RAM;

selecting at least one customized instruction performed by said microprocessor core;

identifying at least one library;

generating a script based at least on said size of said cache, said RAM interface configuration, said at least one customized instruction, and said at least one library; and

running said script to create a customized hardware description language model of the design;

wherein said microprocessor core, said program and data busses, said RAM, and said cache are all physically located on the same die.

59. An integrated circuit, fabricated using the method comprising:

obtaining user input specific to a desired integrated circuit design;

identifying at least one library;

generating a script using at least said user input and said library;

running said script to create a customized description language model of said integrated circuit design;

generating a netlist which is descriptive of the circuitry of said integrated circuit;

compiling said netlist and said hardware description model to produce a compiled integrated circuit design;

compiling at least one configuration file, and

fabricating said integrated circuit using at least said configuration file.

60. A method of designing a configurable processor, the method comprising:

generating a processor specification having a user-definable portion, the user-definable portion of said specification including at least one user-defined instruction having a function associated therewith; and

based on said processor specification, generating a description of a hardware implementation of said configurable processor.

61. The method of Claim 60, wherein said act of generating a description comprises generating a description including control logic necessary for the execution of said at least one user-defined instruction.

62. The method of Claim 61, wherein said act of generating a description of a hardware implementation comprises describing at least an instruction execution pipeline having a plurality of stages, said control logic including portions associated with said stages.

63. The method of Claim 60, wherein said act of generating a description comprises generating a description having at least one element selected from the group consisting of:

(i) registers;

(ii) condition code choices; and

(iii) scratchpad RAM.

64. The method of Claim 60, wherein said act of generating a description comprises generating a description having at least one library of multimedia extensions.

65. The method of Claim 60, further comprising simulating said configurable processor using at least said description.

66. The method of Claim 65, wherein said act of simulating comprises:

running at least one script to generate simulation data;

running at least one simulation using at least said simulation data; and

determining the adequacy of said configurable processor based at least in part on said act of running.

67. The method of Claim 60, further comprising synthesizing said configurable processor using at least said description.

68. The method of Claim 67, wherein said act of synthesizing comprises:

running at least one synthesis script to generate synthesis data;

and evaluating the adequacy of said synthesis data based at least in part on at least one design criterion.

69. The method of Claim 68, wherein said at least one design criterion comprises:

at least one specific processor performance criterion; and

at least one processor die size criterion.

70. The method of Claim 68, further comprising:

revising at least one design element when said act of evaluating indicates that said synthesis data is not adequate;

re-running said at least one synthesis script using said at least one revised design element to generate revised synthesis data;

and re-evaluating the adequacy of said revised synthesis data based at least in part on said at least one design criterion.

71. The method of Claim 70, wherein said at least one design criterion comprises at least one processor die size criterion, and said act of revising comprises revising at least one library.

72. The method of Claim 71, wherein said at least one design criterion comprises at least one processor die size criterion, and said act of revising further comprises revising at least one control file.

73. The method of Claim 70, wherein said at least one design criterion comprises processor clock speed, and said act of revising comprises revising at least one library.

74. The method of Claim 70, wherein said at least one design criterion comprises processor power consumption, and said act of revising comprises revising at least one netlist (net load).